IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Akihiko OTOGURO, et al.**

Serial No.: **Not Yet Assigned**

Filed: **March 7, 2002**

For: **MULTI-LAYERED RESIST STRUCTURE AND MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE**

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

March 7, 2002

Sir:

In compliance with 37 CFR 1.56, Applicants call to the attention of the Patent and Trademark Office the references listed on the attached PTO-1449.

Copies of each of the references are enclosed herewith.

In the event there are any fees due in connection with the filing of this paper, please charge Deposit Account No. 01-2340.

Respectfully submitted,
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Enclosures: References (6)